DATA SHEET

TEA0677T
Dual pre-amplifier and equalizer for reverse tape decks

Product specification
File under Integrated Circuits, IC01

August 1993

Philips Semiconductors

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FEATURES

- Head pre-amplifiers
- Reverse head switching
- Equalization with electronically switched time constants
- 0 dB = 387.5 mV
- Pin compatible to TEA0675 Dolby B, music search IC.

GENERAL DESCRIPTION

The TEA0677T is a monolithic bipolar integrated circuit intended for applications in car radios. It includes head and equalization amplifiers with electronically switchable time constants. Furthermore it includes electronically switchable inputs for tape drives with reverse heads. The device is intended to replace the regular TEA0675T in low-cost car radios using the same PCB. External components that are necessary for Dolby B and music search features can be omitted.

The device will operate with power supplies in the range of 7.6 V to 12.0 V, output overload level increasing with increase in supply voltage. Current drain varies with supply voltage, so it is advisable to use a regulated power supply or a supply with a long time constant.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	7.6	10	12	V
I_{CC}	supply current	–	23	26	mA
(S + N)/N	signal-plus-noise to noise ratio	68	74	–	dB

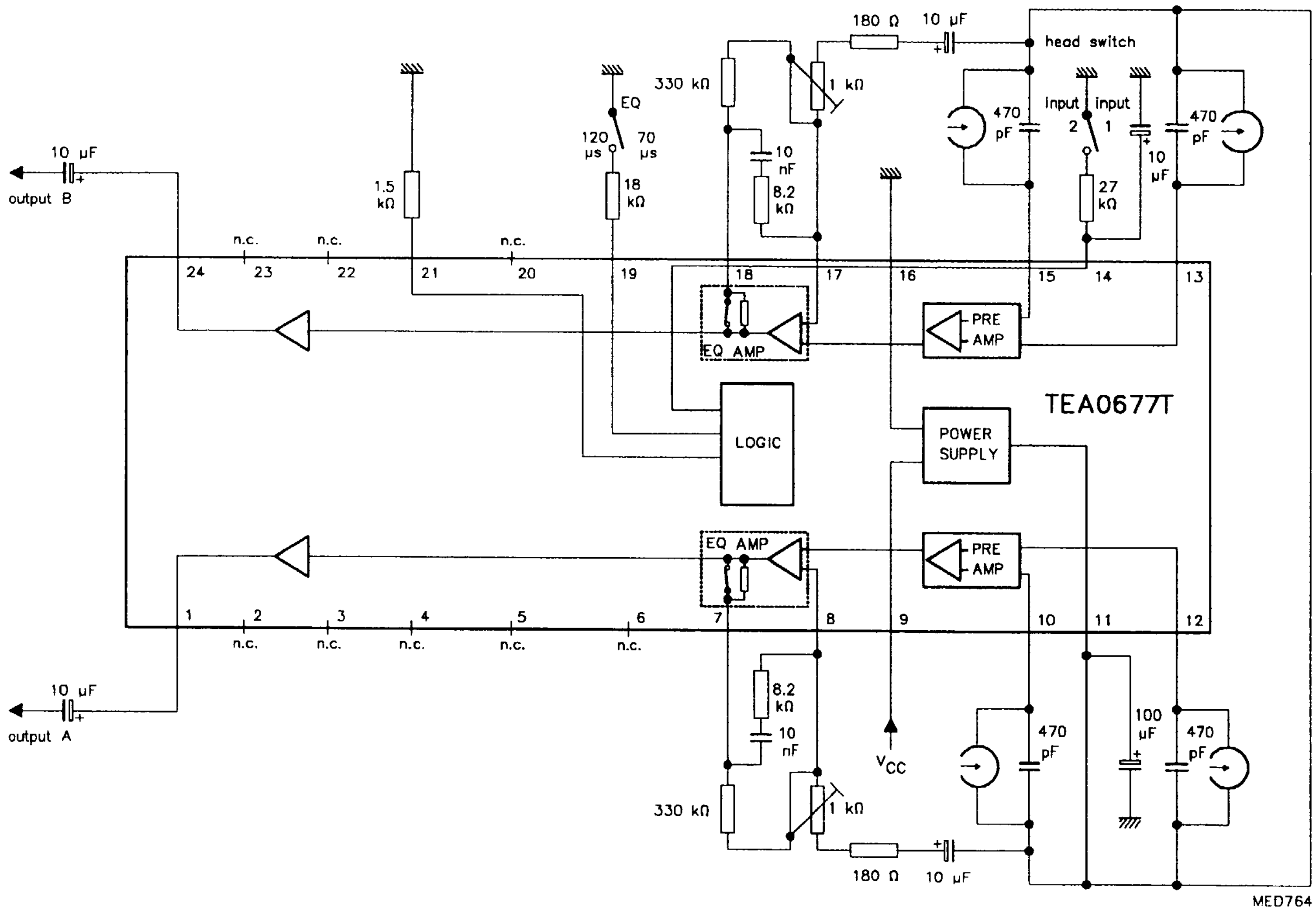
ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA0677T	24	SO	plastic	SOT137A[(1)]

Note

1. SOT137-1; 1996 August 27.

Dual pre-amplifier and equalizer for reverse tape decks



Instead of potentiometers at EQ AMP fixed resistors may be used. The value depends on applied heads.

Fig.1 Block and application diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTA	1	output channel A
n.c.	2	not connected
n.c.	3	not connected
n.c.	4	not connected
n.c.	5	not connected
n.c.	6	not connected
EQA	7	equalizing output channel A
EQFA	8	equalizing input channel A
V_{CC}	9	supply voltage
INA1	10	input channel A1 (forward or reverse)
V_{REF}	11	reference voltage
INA2	12	input channel A2 (reverse or forward)
INB2	13	input channel B2 (reverse or forward)
HS	14	head switch input
INB1	15	input channel B1 (forward or reverse)
GND	16	ground
EQFB	17	equalizing input channel B
EQB	18	equalizing output channel B
EQS	19	equalizing switch input
n.c.	20	not connected
ACUR	21	auxiliary current
n.c.	22	not connected
n.c.	23	not connected
OUTB	24	output channel B

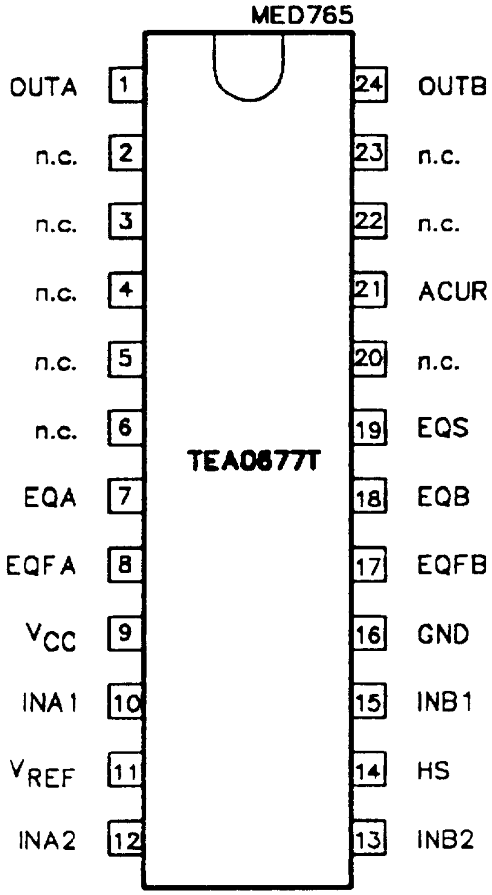


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Head switching is achieved when pin 14 (HS) is connected to GND via a 27 kΩ resistor (inputs INA2, INB2 active), or left open-circuit (inputs INA1, INB1 active). The 10 µF capacitor at pin 14 sets the time constant for smooth switching.

Time constant switching for equalization (70 µs/120 µs) is achieved when pin 19 (EQS) is connected to ground via an 18 kΩ resistor (120µs) or left open-circuit (70 µs).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage	0	16	V
V_I	input voltage (pin 1 to 24) except pin 11 (V_{REF}) to V_{CC}	–0.3	V_{CC}	V
t_{short}	pin 11 (V_{REF}) to V_{CC} short-circuiting duration	–	5	s
T_{amb}	operating ambient temperature	–40	+85	°C
T_{stg}	storage temperature	–65	+150	°C
T_s	soldering temperature (wave solder for 10 s at lead)	–	260	°C
V_{es}	electrostatic handling (note 1)	–	–	–

Note to the Limiting values

1. Classification A: human body model; C = 100 pF, R = 1.5 kΩ, V ≥ 2 kV; charge device model; C = 200 pF, R = 0 Ω, V ≥ 500 V.

CHARACTERISTICS

V_{CC} = 10 V; f = 20 Hz to 20 kHz; T_{amb} = +25 °C; all levels are referenced to 387.5 mV (RMS; 0 dB) at output; see Fig.1; EQ switch in the 70 µs position; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.6	10	12	V
I_{CC}	supply current	pins 10, 12, 13 and 15 connected to V_{REF}	–	23	26	mA
	channel matching	f = 1 kHz; V_O = 0 dB	–0.5	–	+0.5	dB
THD	total harmonic distortion 2nd and 3rd harmonic	f = 1 kHz; V_O = 0 dB	–	0.04	0.1	%
		f = 10 kHz; V_O = 6 dB	–	0.08	0.15	%
	head room at output	V_{CC} = 7.6 V; THD = 1%; f = 1 kHz	12	14	–	dB
PSRR	power supply ripple rejection	0.25 V (RMS); f = 1 kHz; see Fig.3	45	50	–	dB
α_{CS}	channel separation	f = 1 kHz; V_O = +10 dB; see Fig.4	64	70	–	dB
α_{CC}	crosstalk between active and inactive input	f = 1 kHz; V_O = +10 dB	70	77	–	dB
R_{Lmin}	minimum load resistance at output	f = 1 kHz; V_O = 12 dB; THD = 1%	10	–	–	kΩ
G_v	voltage gain (pre-amplifier) from input pins 10, 12, 13 and 15 to pin EQF	f = 1 kHz	29	30	31	dB
V_{off}	input offset voltage		–	2	–	mV
I_B	input bias current		–	0.1	0.4	µA
R_{EQ}	equalizing resistor		4.7	5.8	6.9	kΩ
R_I	input resistance head inputs		60	100	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
A_V	open-loop gain					
	pins INA1/INA2 to pin OUTA	f = 10 kHz	80	86	–	dB
	pins INB1/INB2 to pin OUTB	f = 400 Hz	104	110	–	dB
N	equivalent noise voltage input (RMS value)	unweighted; 20 Hz to 20 kHz; R_{source} = 0 Ω	–	0.7	1.4	μV
(S+N)/N	signal-plus-noise to noise ratio	internal gain 40 dB linear; CCIR/ARM weighted; see Fig.4	68	74	–	dB
	DC output voltage; pins 1 (OUTA) and 16 (OUTB)	reference to $V_{REF;}$ tape head DC coupled	–	–	±0.15	V
I_{OGND}	DC output current capability	to ground	–2	–	–	mA
I_{OVCC}	DC output current capability	to V_{CC}	300	–	–	μA
Z_O	output impedance		–	80	100	Ω
Switching thresholds						
Equalization (pin 19)						
V_{EQS}	voltage at pin EQS		–	–	5	V
I_{EQ70}	70 μs input current		–	–	–150	μA
I_{EQ120}	120 μs input current		–250	–	–1000	μA
Head switch (pin 14)						
V_{IN1}	inputs INA1 and INB1 active	note 1	$0.65V_{CC}$	$0.775V_{CC}$	$1.0V_{CC}$	V
I_{IN1}	maximum input current		–150	90	150	μA
V_{IN2}	inputs INA2 and INB2 active		$0.1V_{CC}$	$0.225V_{CC}$	$0.35V_{CC}$	V
I_{IN2}	maximum input current		–50	–90	–150	μA

Note to the characteristics

1. For an application with a fixed EQ time constant of 120 μs the equalizing network may be applied completely external. In this application the 8.2 kΩ resistor has to be changed to 14 kΩ and the internal resistor R_{EQ} = 5.8 kΩ must be short-circuited by fixing the EQ-switch input at the 70 μs position (pin 19; EQS left open-circuit). To activate the inputs INA1 and INB1 pin 10 (HS) may be left open-circuit. In this event the DC level at pin 10 (HS) is 0.775 V_{CC}.

General note

It is recommended to switch off V_{CC} with a gradient of 400 V/s at maximum to avoid plops on tape in the event of contact between tape and tape head while switching off.

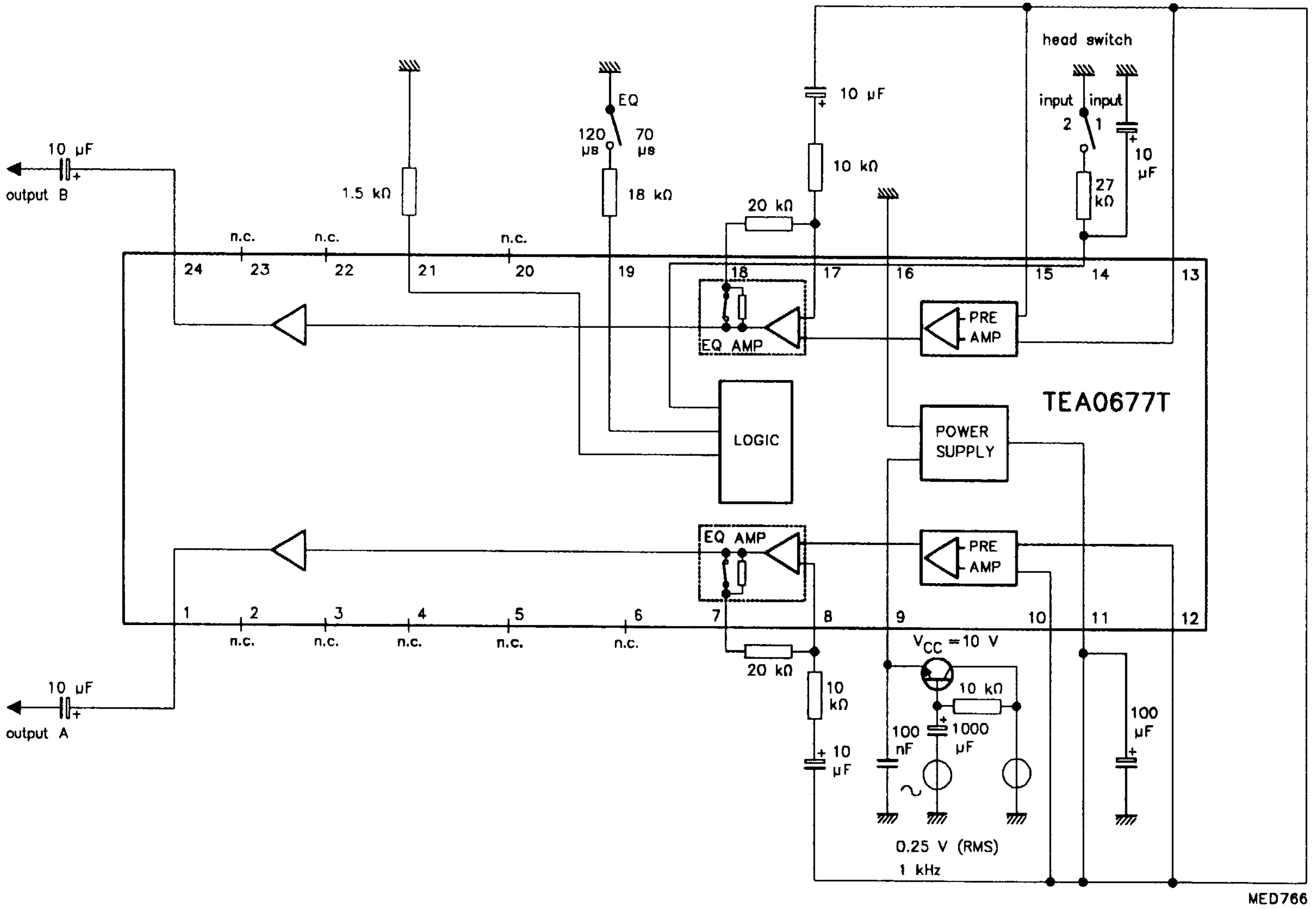


Fig.3 Test circuit for power supply ripple rejection.

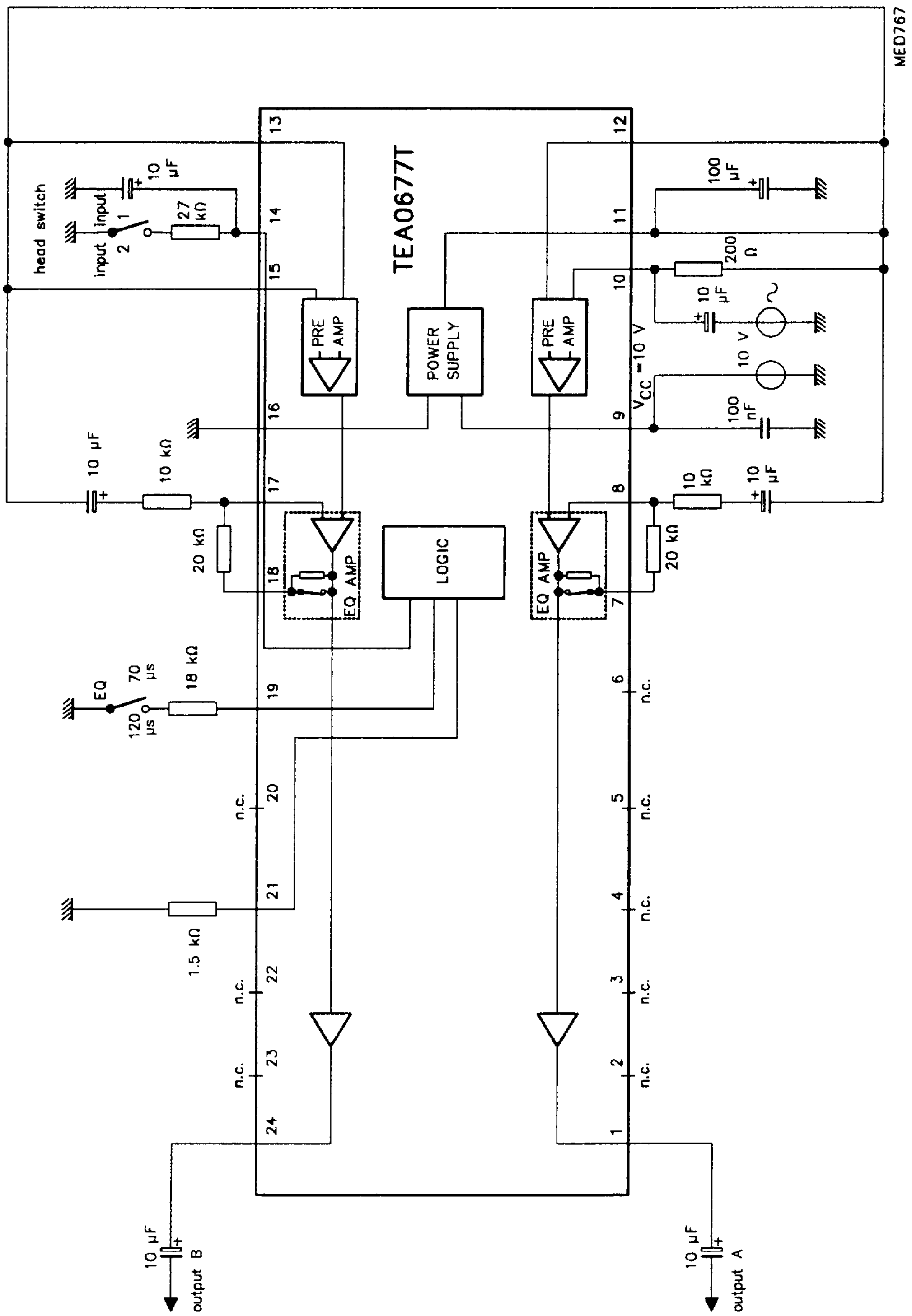


Fig.4 Test circuit for channel separation and signal-to-noise ratio.

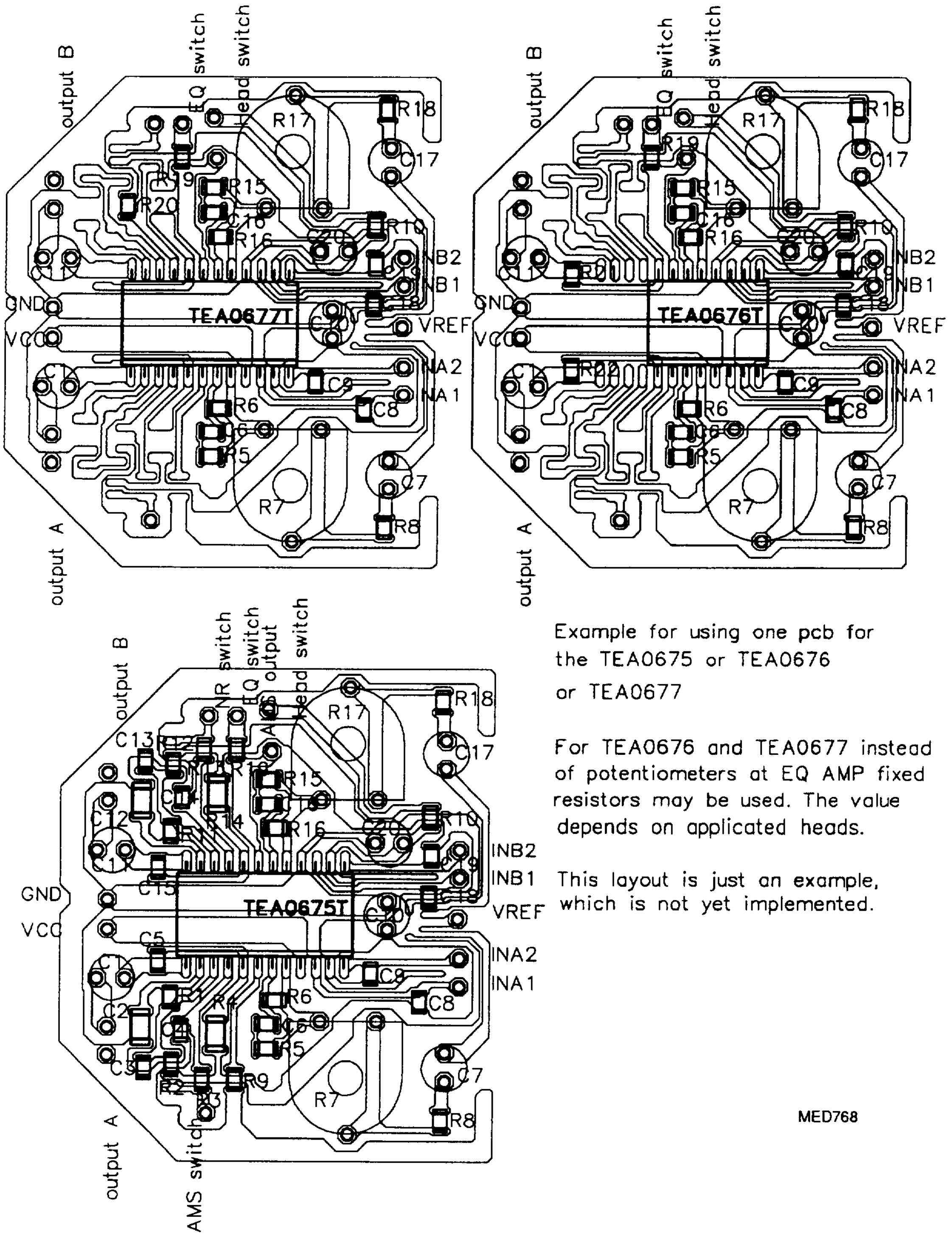


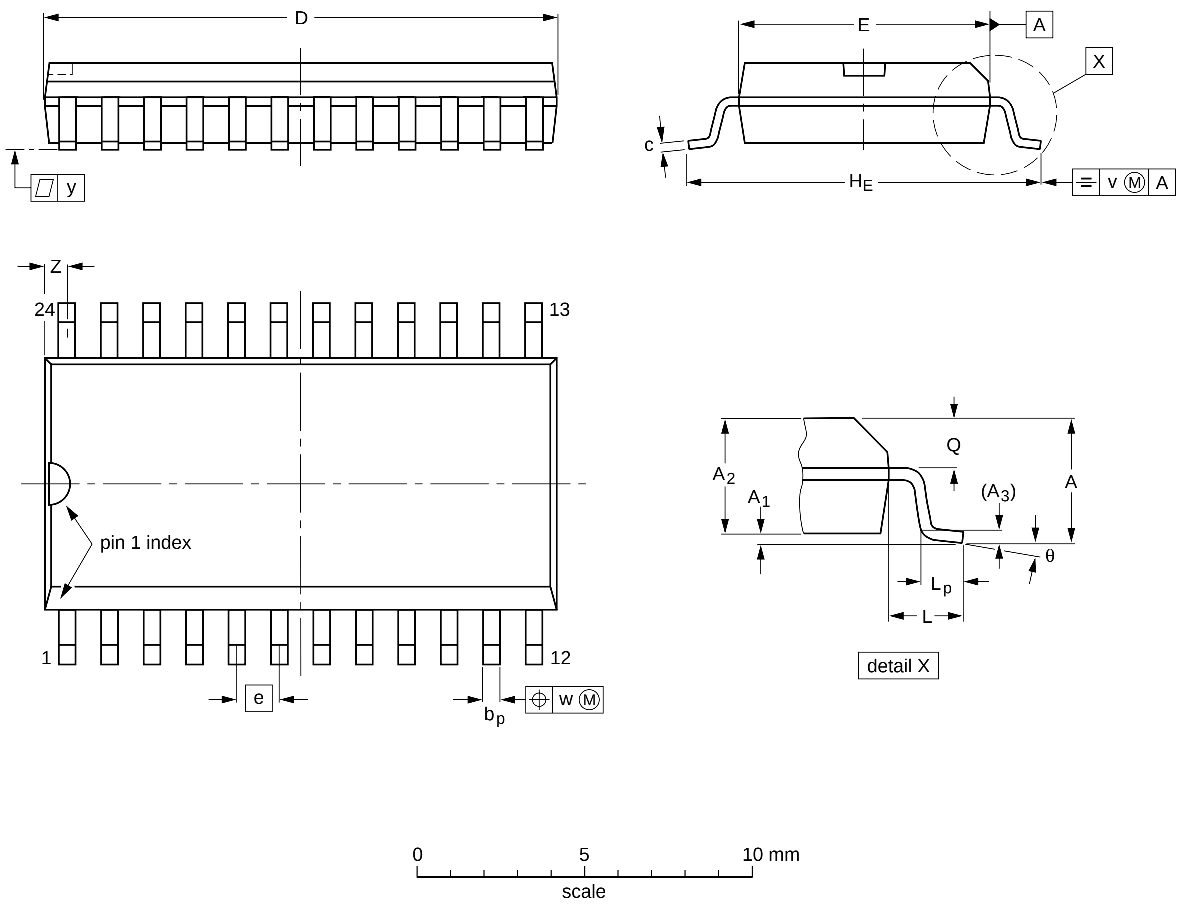
Fig.5 PCB layout example.

Table 1 Component list pcb layout example.

COMPONENT	VALUE
R1, R11	270 kΩ
R2, R12	180 kΩ
R3, R13, R20	1.5 kΩ
R4, R14	24 kΩ
R5, R15	8.2 kΩ
R6, R16	330 kΩ
R7, R17	1 kΩ
R8, R18	0.18 kΩ
R9	68 kΩ to 1000 kΩ
R10	27 kΩ
R19	18 kΩ
R21, R22	0 kΩ
C1, C11, C7, C17, C20	10 µF
C2, C12	330 nF
C3, C13	100 nF
C4, C14	15 nF
C5, C15	4.7 nF
C6, C16	10 nF
C8, C9, C18, C19	0.47 nF
C10	100 µF

PACKAGE OUTLINE

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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